REMARKS

Claims 8-11, 17-19, 21, 24 and 25 have been rejected under 35 U.S.C. 102(b) as being anticipated by Manning et al. (U.S. Patent No. 5,909,617). Claims 8-18 have been canceled, thereby rendering the rejection of these claims moot.

Claim 19 recites "a continuous silicide strap directly contacting the conductive element, the dielectric spacer and the semiconductor substrate."

In contrast, Manning et al. teaches that a polysilicon layer 80 is deposited over the gate 76, the adjacent sidewall spacer and the drain 78 (Manning et al., Col. 7, lines 5-12; Fig. 9.) Regions 94 of polysilicon layer 80 are subsequently doped. (Manning et al., Col. 7, lines 30-32; Fig. 11.) Metal layer 100, most preferably titanium, is deposited over polysilicon region 94. (Manning et al., Col. 7, lines 53-55; Fig. 12.) The structure is then sintered, such that the titanium reacts with the adjacent polysilicon region 94 to form silicide 110. (Manning et al., Col. 7, lines 58-62; Fig. 13.) For example, a silicide strap 114 electrically connects the gate 76 and drain 78. (Manning et al., Col. 8, lines 11-12.) However, unreacted portions of the polysilicon region 94 remain after the sintering step. (See, Manning et al., Fig. 13; Col. 8, lines 5 and 8-10.)

Because Manning et al. teaches that unreacted portions of the polysilicon region 94 remain between the silicide strap and the gate 76, the sidewall spacer and the drain 78, Manning et al. fails to teach a "silicide strap directly contacting the conductive element, the dielectric spacer and the semiconductor substrate" as recited by Claim 19.

For these reasons, Claim 19 is not anticipated by Manning et al.

Claim 21 recites "a semiconductor region dispersed in the upper surfaces of the conductive element, the dielectric spacer and the semiconductor substrate; and a silicide strap formed in the semiconductor region."

As described above, Manning et al. teaches that a polysilicon layer 80 is deposited over the gate 76, the adjacent sidewall spacer and the drain 78. (Emphasis added.) Thus, the polysilicon layer 80 is not "a semiconductor region dispersed in the upper surfaces" as recited by Claim 21.

For these reasons, Claim 21 is not anticipated by Manning et al. Claims 24 and 25, which depend from Claim 21, are not anticipated by Manning et al. for at least the same reasons as Claim 21.

In addition, Claim 24 recites, "the semiconductor region comprises an implanted semiconductor layer". (Emphasis added.) The Examiner indicates that polysilicon layer 80 of Manning et al. teaches "an implanted semiconductor layer" as recited by Claim 24. However, Manning et al. explicitly teaches that "polysilicon layer 80 is deposited conformally", wherein "chemical vapor deposition (CVD) is preferred for this deposition" (Manning et al., Col. 7, lines 5-8.) Thus, polysilicon layer 80 of Manning et al. is not "an implanted semiconductor layer" as recited by Claim 24, but rather, a deposited semiconductor layer. For this additional reason, Claim 24 is not anticipated by Manning et al. Claim 25, which depends from Claim 24, is additionally allowable for at least the same reasons as Claim 24.

Claims 12-16, 20, 22 and 23 have been rejected under 35 U.S.C. 103(a) as being anticipated by Manning et al. Claims

12-16 have been canceled, thereby rendering the rejection of these claims moot.

Claim 20, which depends from independent Claim 19, is allowable over Manning et al. for at least the same reasons as Claim 19.

Claim 22, which depends from independent Claim 21, is allowable over Manning et al. for at least the same reasons as Claim 21.

Claim 23, which depends from independent Claim 21, is allowable over Manning et al. for at least the same reasons as Claim 21. In addition, Claim 23 recites "the semiconductor region comprises amorphous silicon". Because Manning et al. does not teach or suggest "a semiconductor region dispersed in the upper surfaces of the conductive element, the dielectric spacer and the semiconductor substrate" as recited by Claim 21, it is not obvious for such a semiconductor region to have a certain composition, such as "amorphous silicon", as recited by Claim 23.

Applicants have added new Claims 26-38. Support for these new claims is found throughout the specification as originally filed.

CONCLUSION

Claims 19-38 are pending in the present application. Reconsideration and allowance of these claims is respectfully requested. If the Examiner has any questions or comments, he is invited to call the undersigned at (925) 895-3545.

Respectfully submitted,

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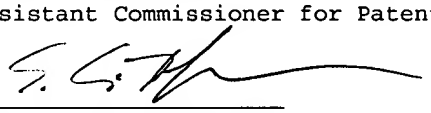

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